CLAIMS

1. An active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element (2);

an amorphous silicon drive transistor (T_D) for driving a current through the display element;

first and second capacitors (C_1, C_2) connected in series between the gate and source or drain of the drive transistor, a data input to the pixel being provided to the junction between the first and second capacitors (C_1, C_2) thereby to charge the second capacitor (C_2) to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor (C_1).

2. A device as claimed in claim 1, wherein each pixel further comprises an input first transistor (A_1) connected between an input data line (32) and the junction between the first and second capacitors (C_1, C_2).

3. A device as claimed in claim 1 or 2, wherein the drain of the drive transistor (T_D) is connected to a power supply line (26).

4. A device as claimed in any preceding claim, wherein each pixel further comprises a second transistor (A_2) connected between the gate and drain of the drive transistor

5. A device as claimed in claim 4, wherein the second transistor (A_2) is controlled by a first gate control line which is shared between a row of pixels.

6. A device as claimed in any preceding claim, wherein the first and second capacitors (C_1, C_2) are connected in series between the gate and source of the drive transistor (T_D).

7. A device as claimed in claim 6, wherein each pixel further comprises a third transistor (A_3) connected across the terminals of the second capacitor (C_2).

8. A device as claimed in claim 7, wherein the third transistor is controlled by a third gate control line which is shared between a row of pixels.

9. A device as claimed in claim 8, wherein the second and third gate control lines comprise a single shared control line.

10. A device as claimed in any one of claims 1 to 5, wherein the first and second capacitors (C_1, C_2) are connected in series between the gate and drain of the drive transistor (T_D).

11. A device as claimed in claim 10, wherein each pixel further comprises a third transistor (A_3) connected between the input and the source of the drive transistor (T_D).

12. A device as claimed in claim 11, wherein the third transistor (A_3) is controlled by a third gate control line which is shared between a row of pixels.

13. A device as claimed in claim 12, wherein the second and third gate control lines comprise a single shared control line.

14. A device as claimed in any preceding claim, wherein each pixel further comprises a fourth transistor (A_4) connected between the drive transistor source and a ground potential line.

15. A device as claimed in claim 14, wherein the fourth transistor (A_4) is controlled by a fourth gate control line which is shared between a row of pixels.

16. A device as claimed in claim 15, wherein the ground potential line is shared between a row of pixels and comprises the fourth gate control line for the fourth transistors of an adjacent row of pixels.

17. A device as claimed in claim 1 or 2, wherein the capacitor arrangement (C_1, C_2) is connected between the gate and source of the drive transistor (T_D), and the source of the drive transistor is connected to a ground line.

18. A device as claimed in claim 17, wherein the drain of the drive transistor (T_D) is connected to one terminal of the display element (2) the other terminal of the display element being connected to a power supply line.

19. A device as claimed in claim 17 or 18, wherein each pixel further comprises a second shorting transistor (A_2) connected across the terminals of the second capacitor (C_2).

20. A device as claimed in any one of claims 17 to 19, wherein each pixel further comprises a third transistor (A_3) connected between the gate and drain of the drive transistor.

21. A device as claimed in claim 20, wherein the third transistor (A_3) is controlled by a gate control line which is shared between a row of pixels.

22. A device as claimed in any one of claims 17 or 21, wherein each pixel further comprises a fourth charging transistor (A_4) connected between a power supply line (50) and the drain of the drive transistor.

23. A device as claimed in any one of claims 1 to 16, wherein each pixel further comprises a second drive transistor (T_S).

24. A device as claimed in claim 23, wherein the second drive transistor is provided between a power supply line (26) and the first drive transistor (T_D).

25. A device as claimed in claim 24, wherein the gate and drain of the second drive transistor are connected together.

26. A device as claimed in claim 23, wherein the second drive transistor is provided between the first drive transistor (T_D) and the display element (2).

27. A device as claimed in claim 26, wherein a transistor (A_5) is connected between the gate and drain of the second drive transistor (T_S).

28. A device as claimed in claim 26 or 27, wherein each pixel further comprises a fourth transistor (A_4) connected between the gate of the second drive transistor (T_S) and a ground potential line.

29. A device as claimed in any preceding claim, wherein the drive transistor (T_D) comprises an n-type transistor.

30. A device as claimed in any preceding claim, wherein the display element comprises an electroluminescent (EL) display element.

31. A device as claimed in claim 30, wherein the electroluminescent (EL) display element comprises an electrophosphorescent organic electroluminescent display element.

32. A method of driving an active matrix display device comprising an array of current driven light emitting display pixels, each pixel comprising an display element (2) and an amorphous silicon drive transistor (T_D) for driving a current through the display element, the method comprising, for each pixel:

driving a current through the drive transistor (T_D) to ground, and charging a first capacitor (C_1) to the resulting gate-source voltage;

discharging the first capacitor (C_1) until the drive transistor turns off, the first capacitor thereby storing a threshold voltage;

charging a second capacitor (C_2) , in series with the first capacitor between the gate and source or drain of the drive transistor, to a data input voltage; and

using the drive transistor (T_D) to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors (C_1, C_2).

33. A method as claimed in claim 32, wherein the step of charging a second capacitor is carried out by switching on an address transistor (A_1) connected between a data line and an input to the pixel.

34. A method as claimed in claim 33, wherein the address transistor for each pixel in a row is switched on simultaneously by a common row address control line.

35. A method as claimed in claim 34, wherein the address transistors for one row of pixels are turned on substantially immediately after the address transistors for an adjacent row are turned off.

36. A method as claimed in claim 32, wherein the first capacitor (C_1) of each pixel is charged to store a respective threshold voltage of the pixel drive transistor at an initial threshold measurement period of a display frame period, a pixel driving period of the frame period following the threshold measurement period.